This listing of claims will replace all prior versions, and listings, of claims in the application:

The Status of the Claims

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Original) A method to fabricate a semiconductor device, the method comprising:

forming an uppermost metal interconnect on a semiconductor substrate;

forming an oxide layer on the substrate and the uppermost metal interconnect;

forming an aluminum layer on the oxide layer; and

forming a stress-relief layer on the aluminum layer to reduce stress on the metal interconnect.

7. (Original) A method as defined in claim 6, wherein forming the stress-relief layer comprises:

performing a plasma treatment on a surface of the aluminum layer to form an aluminum oxide layer; and

annealing the aluminum oxide layer.

8. (Original) A method as defined in claim 7, wherein the plasma treatment uses at least one of N_2O gas and O_2 gas.

9. (Original) A method as defined in claim 7, wherein the annealing is performed at a temperature of 200 to 400℃.

10. (Original) A method as defined in claim 7, wherein the aluminum oxide layer is annealed in an atmosphere of inert gas.

11. (Original) A method as defined in claim 10, wherein the inert gas is at least one of Ar and He.

12. (Original) A method as defined in claim 8, wherein the aluminum oxide layer is annealed in an atmosphere of inert gas.

13. (Original) A method as defined in claim 7, wherein the aluminum oxide layer is annealed in an atmosphere of gas including at least one of N_2O, O_2, N_2, and H_2.

14. (Original) A method as defined in claim 8, wherein the aluminum oxide layer is annealed in an atmosphere of gas including at least one of N_2O, O_2, N_2, and H_2.

15. (Original) A method as defined in claim 6, wherein the semiconductor device is at least one of a multi-interconnect adapted device and a power device.